Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) Apparatus, comprising:

a digital data channel which stores input data to a data storage medium and subsequently retrieves output data from the medium made from the input data; and

a circuit connected to the digital data channel which can characterize the stored input data and the retrieved output data in at least two alternative digital configurations and predict error rate performance in relation to a first of the alternative digital configurations for both the input data and output data and, alternatively, to a second of the alternative digital configurations for both the input data and output data.

2. (Previously presented) The Apparatus of claim 1, wherein the input data is characterized as an input sequence of multibit symbols each having a first selected symbol length and the output data is characterized as an output sequence of multibit symbols each having the first selected symbol length.

3. (Previously presented) The Apparatus of claim 2 wherein the circuit characterizes the input data into a second input sequence of multibit symbols each having a second selected symbol length different from the first selected symbol length and operates to arrange

the output data into a second output sequence of multibit symbols each having the second selected symbol length.

4. (Previously presented) The apparatus of claim 1, wherein the circuit predicts the error rate performance in relation to only one digital configuration of the input and output data.

5. (Previously presented) The apparatus of claim 1, wherein the circuit performs run length limited (RLL) encoding upon the input data prior to characterizing the input data, and wherein the circuit further inhibits RLL decoding of the output data to reflect said RLL encoding.

6. (Previously presented) The apparatus of claim 1, wherein the circuit determines the number of errors in the output data in relation to a preselected number of errors that can be corrected by a first error correction code (ECC) encoding methodology.

7. (Previously presented) The apparatus of claim 1, wherein the circuit arranges the input data into a plurality of interleaves and arranges the output data into a corresponding plurality of interleaves.

8. (Previously presented) The apparatus of claim 1, wherein the circuit concurrently inhibits and emulates selected operation of the digital data channel.

9. (Previously presented) The apparatus of claim 2 wherein the circuit determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence.

10. (Previously presented) The apparatus of claim 3 wherein the circuit determines a number of erroneous symbols in the second output sequence in relation to differences between the second input sequence and the second output sequence.

11. (Previously presented) The apparatus of claim 1 wherein the circuit predicts the error rate performance in relation to two or more digital configurations of the input and output data.

12. (Previously presented) The apparatus of claim 2 wherein the circuit comprises a symbol comparator circuit comprising a plurality of state machines each configured to arrange a selected set of data into a selected number of different symbol lengths.

13. (Previously presented) The apparatus of claim 12, wherein the symbols of the input sequence and the output sequence are respectively arranged into corresponding pluralities of interleaves, and wherein the circuit further comprises an interleave counter circuit which determines an uncorrectable number of erroneous symbols in each interleave that exceed a correctable number of erroneous symbols that can be detected by a first ECC encoding methodology.

14. (Canceled)

15. (Currently amended) Method, comprising:

using a digital data channel to store input data to a data storage medium;

subsequently using the digital data channel to obtain output data from the medium;

after storing the input data in the using step, arranging the input data into a selected digital configuration from a plurality of different selectable digital configurations;

arranging the output data into the selected digital configuration; and

comparing the output data arranged in the selected digital configuration with the input data arranged in the selected digital configuration to determine an error rate performance.

16. (Previously presented) The method of claim 15 wherein the comparing step is characterized by using a first error correction code (ECC) encoding methodology based on the selected digital configuration.

17. (Previously presented) The method of claim 16, wherein the comparing step is characterized by determining a number of errors in the output data in relation to a selected number of errors that can be detected by the first error correction code (ECC) encoding methodology.

18. (Previously prescnted) The method of claim 15, wherein thc arranging the input and output data steps arc characterized by sequences of multibit symbols each having a selected symbol length.

19. (Previously presented) The method of claim 18 wherein the arranging the input and output data steps are characterized by sequences of multibit symbols each having a second selected symbol length.

20. (Previously prescnted) The method of claim 19 wherein thc comparing step is characterized by predicting error rate performance using a second error correction code (ECC) encoding methodology based on the second selected symbol length.

21. (Previously presented) The method of claim 15 wherein the arranging the input and output data steps are characterized by performing run length limited (RLL) encoding upon the input data and inhibiting RLL decoding of the output data to reflect said RLL encoding.

22. (Previously presented) The method of claim 15, wherein thc arranging thc input and output data steps are characterized by arranging the data into a plurality of interleaves.

23. (Previously presented) Thc method of claim 15 comprising concurrently inhibiting and emulating selected operation of the digital data channel.

24. (Previously presented) The method of claim 15 wherein the comparing step is characterized by predicting the error rate in relation to only one selected digital configuration of the input and output data.

25. (Previously presented) The method of claim 15 wherein the comparing step is characterized by predicting the error rate in relation to two or more selected digital configurations of the input and output data.

26. (Previously presented) The method of claim 18 wherein the comparing step is characterized by predicting the error rate in relation to differences between the input sequence and the output sequence.

27. (Canceled)

28. (Currently amended) A data storing and retrieving apparatus, comprising:

a digital data channel capable of storing input data to a storage medium and retrieving output data from the medium; and

means for predicting error rate performance in relation to a selected digital data configuration of a plurality of different digital data configurations for both the same input data and the same output data.

29. (Currently amended) [[A]] An emulation system comprising a circuit for predicting error rate performance associated with storing data and retrieving the stored data,

the circuit configured for comparing stored data with retrieved data after characterizing both the stored data and the retrieved data in a selected digital configuration from a plurality of different selectable digital configurations.

30. (Currently amended) A method comprising:

characterizing stored data in a selected digital configuration from a plurality of selectable digital configurations[[, and]];

characterizing retrieved data from the stored data in the selected digital configuration[[,]]; and

comparing the characterized data in order to predict an error rate performance associated with storing and retrieving the data.